

## DATASHEET

# UMC-Synopsys 65nm Low Power UPF Reference Flow

The UMC-Synopsys Low Power UPF Reference Flow provides a top-down solution from RTL to GDSII in the Synopsys Eclipse™ low power solution, which fully supports the industry leading standard Unified Power Format (UPF).

This hierarchical flow not only resolves phenomenon encountered with UMC's 65nm process and IPs, but also eliminates many potential issues that may arise from low-power design strategies.

As such, this low power UPF flow is intended to adapt to any customer design environment by using the highly flexible and configurable LEON-2 processor as its core to exercise its flow steps.

It also offers a robust means to help increase our customers' SoC design competitiveness by accelerating their time-to-silicon and avoiding pricey re-spins. This design flow is segmented into five comprehensible phases with UPF: Synthesis, DFT, Floorplan, Place & Route, DFM optimization, and Chip Finishing.

### Phase 1: Synthesis

In this stage, the Top-Down low power aware synthesis is done. The power domain is created to effectively manage the power information of cell libraries. Meanwhile, the **Level Shifter (LS)** and **Isolation (ISO)** cells are inserted to the nets, which connected the cells within different power domains. The **Retention Register (RR)** cell mapping is also performed.

### Phase 2: Design For Test (DFT)

In this stage, power domain aware scan chain insertion will be performed and insert **ISO** cell and **LS** cell for test pins within cross power domain.

### Phase 3: Floorplan

In this stage, floorplan is performed with voltage area creation, **Tap cell & Power Switch (PS)** cell placement and multiple-voltage power network creation.

### Phase 4: Place & Route

In this stage, P&R is performed with timing closure and low power consumption. **PS** cells are automatically handled and arranged in this phase. A sequence of actions is then conducted to complete time-driven placement, scan chain reordering, clock tree synthesis, time-driven routing, post-route optimization, and DFM optimization are some of the steps.

### Phase 5: Chip Finishing

The final stage refines the full chip implementation to achieve timing/power analysis, multi-voltage rule checking, formal checking and function verification. Finally the tapeout-ready GDS file will be ready.

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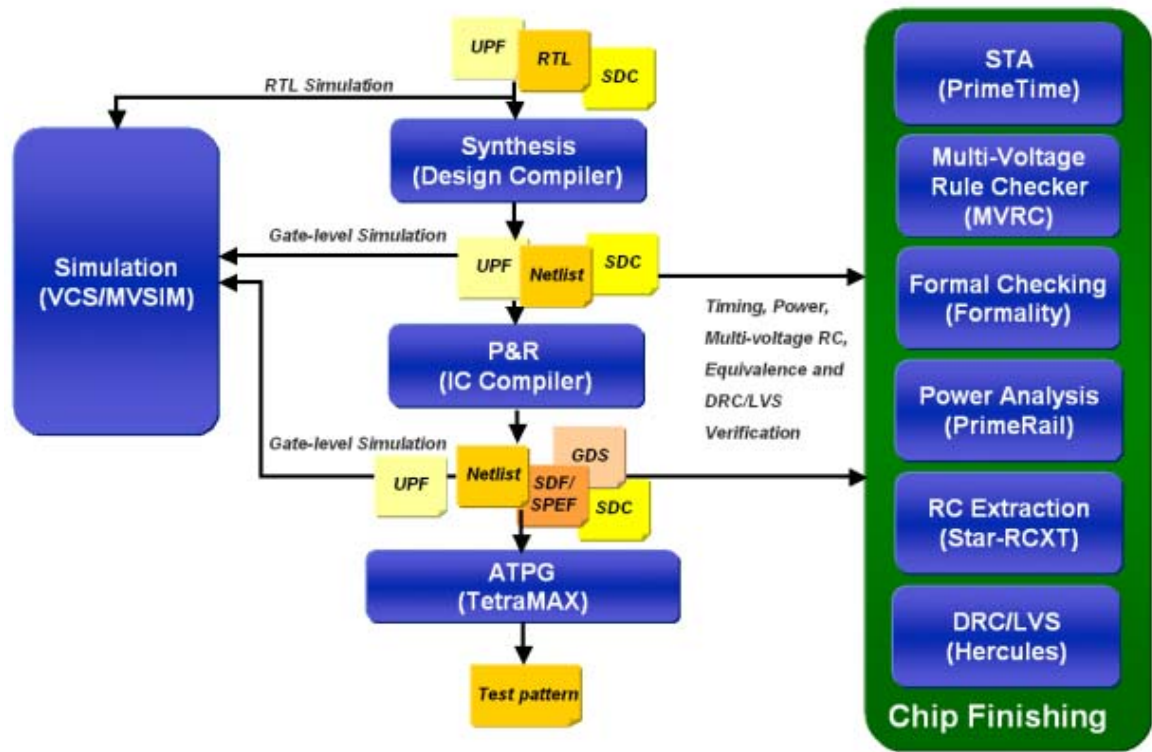


Figure 1. Overview of UMC-Synopsys Low Power UPF Reference Flow